FABRICATION METHOD AND STRUCTURE FOR A DRAM CELL WITH BIPOLAR CHARGE AMPLIFICATION

This a division of patent application Ser. No. 08/963,457, filing date Nov. 3, 1997, now U.S. Pat. No. 5,872,032, A New Fabrication Method And Structure For A Dram Cell With Bipolar Charge Amplification, assigned to the same assignee as the present invention.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the dynamic random access memories (DRAM) and more particularly to the structures and methods of fabrication of DRAM's with charge amplification.

2. Description of Related Art

The fabrication and structure of DRAM cells and DRAM array are well known in the art. Typical cell structures for high density DRAM in prior art is composed of one transistor M1 **10** for switching charges and one storage capacitor C **15** for storing charges as illustrated in FIG. **1***a*. The transistor M1 **10** will be an n-MOS transistor fabricated in a triple well as shown in FIG. **1***b*. A deep N-well **35** will be formed in a p-type substrate **30**. The area for the deep n-well **35** will be formed as openings during the formation of the insulation are by the local oxidation of the silicon substrate (LOCOS) **45**. Within the deep n-well **35** a shallower p-well well **40** will be formed. The gate **60** of the n-MOS transistor M1 **10** will be formed as a conductive material such as polysilicon placed over an insulating gate oxide **55** to define the channel area that will between the drain **50** and source **80** of the n-MOS transistor M1 **10**.

The capacitor C **15** is formed by placing a conductive metal connected to the substrate biasing voltage source V_{ss} **75** on a dielectric **70** placed over the N^+ drain **80** of the transistor M1 **10**. The capacitor C **15** as shown is diagrammatic. The particular structure of the capacitor C **15** is well known and shown in "The Evolution Of DRAM Cell Technology" by B. El-Kareh et al., Solid State Technology, May 1997, pp. 89–101. In order to maintain the minimum storage capacitance of 30–40 fF of a cell, the structure of the DRAM cell results in complex semiconductor processing to develop these structures.

A corresponding DRAM cell using p-MOS transistor can certainly be used with polarity and operation bias reversed accordingly.

The deep n-well **35** is typically biased to the power supply voltage source V_{cc} (i.e. the highest potential on chip) and the p-well is biased to substrate biasing voltage source V_{ss} **75** (i.e. the lowest voltage on chip). The substrate biasing voltage source V_{ss} **75** may be biased below ground (i.e. negative potential) so that the leakage current through the pass transistor M_1 **10** is reduced. The presence of charge in the storage capacitor C **15** indicates a logical "1" and its absence of charge indicates a logical "0". The storage capacitor C **15** is connected to n+drain **80** of the transistor M_1 **10**, and the other n+ source **50** of the transistor M_1 **10** is connected to bit-line V_{bit} **25** that controls the reading and writing of the DRAM cell. The gate of the MOS transistor M1 **10** is connected to the word line V_{word} to control the selection of the DRAM cell.

The DRAM cells Cell **11 200**, Cell **12 205**, Cell **21 210**, Cell **22 215** are arranged in arrays of rows (word-lines WL**0**, WL**1**, WL**2**, and WL**3**,) and columns (bit-lines or BL**0** and BL**1**) as shown in FIG. **2**. One popular DRAM array is the folded bit-line architecture. Each pair of bit-lines BL**0** and BL**1** is connected to one sense amplifier **220** where one Bit-lines BL**0** or BL**1** serves as reference bias and the other BIT-LINES BL**0** or BL**1** serves as bit-line sensing during read operation. During write operation, the bit-line BL**0** and BL**1** is charged to either V_{cc} to write a logical "1" or V_{ss} to write a logical "0". The selected word-line WL**0**, WL**1**, WL**2**, or WL**3** is charged to V_{cc} so that all transistors connected to the same row turn on and the capacitor of each cell are charged to V_{cc} or V_{ss} representing information of "1" and "0" respectively. Before read operation starts, the bit-lines BL**0** and BL**1** are precharged to a voltage $V_{cc}/2$. To start reading a cell, the selected word-line WL**0**, WL**1**, WL**2**, or WL**3** is raised to V_{cc}, turning on all transistors connected to the word-line WL**0**, WL**1**, WL**2**, or WL**3**. Each sense amplifier **220** detects the polarity of charge stored on capacitor C with respect to the reference Bit-lines BL**0** and BL**1** voltage (i.e. $V_{cc}/2$).

The signal appearing at the input of sense amplifier **220** is very small (~100–200 mv), since the cell capacitance is small (<10%) compared to the bit-line capacitance. Throughout generations of DRAM, the minimum storage capacitance C needs to be 30–40 fF as described above in order to maintain read performance.

The requirement of large storage capacitance of conventional one-transistor cell results in high and multi-layered stack or deep trench capacitors, which is one of the major scaling limits in DRAM technology. Therefore, there is a need for innovations for reducing the requirement of storage capacitance in DRAM cell. One DRAM cell of the prior art adds a bipolar transistor to the DRAM cell for charge amplification as shown in FIG. **3***a*. DRAM cells with charge amplification are disclosed in U.S. Pat. No. 4,677,589 (Haskell et al.) and U.S. Pat. No. 5,363,325 (Sunouchi et al.) and shown in FIG. **3***a* and **3***b*. The structure of the cell is similar to that of FIGS. **1***a* and **1***b*. The n-MOS transistor M1 **300** acts to switch the charges to and from the capacitor C **315**. However, transistor Q1 **310** acts to amplify the signal developed by the charges present on the capacitor to allow smaller charges to be present and still detect the logical "1" or the logical "0". The write of a logical "1" occurs when the bit-lines V_{bit} **320** is brought to the voltage level V_{cc}. This will allow the p/n junction formed by the emitter-base **350** of the bipolar transistor Q1 **310** to conduct thus charging the capacitor C **305** to nearly the value of the power supply voltage source V_{cc}.

When the cell is to be written to logical "0", the bipolar transistor Q1 **310** will be nonconducting and any charge present on the capacitor C **305** will have to leak through parasitic paths from the capacitor C **315**. This will cause the writing of a logical "0" to be very slow.

The structure of the bipolar transistor Q1 **310** is formed by diffusing a p^+ emitter **352** in the area that forms the N source of the n-MOS transistor M1 **300**. The bipolar transistor Q1 **310** is thus formed as a merged transistor with the n-MOS transistor M1 **300** by the p^+ emitter **352**, the N-base **350** (also the source of the n-MOS transistor M1 **300**), and the p-well **340** that acts as the collector.

"A Complementary Gain Cell Technology For Sub-1 v Supply Dram's", Shukuri et al., Digest of IEDM, p. 1006, 1992 and "Super-Low-Voltage Operation Of Semi-Static Complementary Gain DRAM Memory Cell", Shukuri et al., Digest of VLSI Technology Symposium, p. 23, 1993 describes a DRAM cell incorporating charge amplification. A complementary cell that has an n-MOS transistor and a